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Design of Low Voltage Low Power OTA based CCII+

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ABSTRACT

This paper presents a design of low power low voltage positive second generation current conveyor (CCII) which is based on Miller compensated Operational Transconductance Amplifier (OTA). The OTA realisation is carried out using low power techniques bulk-driven (BD) and bulk-driven quasi-floating gate (BDQFG) for a comparison of aforementioned techniques. The use of bulk-driven approach facilitates the proposed CCII design operable at sub-volt supply. Furthermore, CCII realisations using BD and BDQFG have been done so as to have a fair comparison of advantage of using BDQFG over BD in terms of improving transconductance and frequency response. The proposed CCII operates at 0.4V. The complete analysis has been carried out in 0.18 μm CMOS technology with the help of HSpice simulator.

Keywords: Bandwidth, Bulk Driven, Current conveyor, Floating gate, Impedance, Quasi-floating gate

INTRODUCTION

Low power, low cost and maintenance-free precise medical equipment mainly used in long-term monitoring applications have become a difficult task in deep submicron technologies. In analog circuits, the short channel effect (SCE) results in an offset and also decreased output impedance. Proportional to technology scaling, the supply voltage is also scaled but this limits threshold voltage of MOS transistor which is not scalable proportionally (Blalock, Allen, & Rincon-Mora, 1998). To resolve the threshold voltage issue, techniques such as bulk-driven (BD), sub-threshold operation, level shifter, floating and quasi floating gate (FG and QFG), and recently reported bulk-driven floating and quasi-floating gate (BDFG and BDQFG) have been reported to achieve low power dissipations (Khateb, Dabbous, & Vlassis, 2013; Raj, Singh, & Gupta,

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2015; Raj & Gupta, 2015). The bulk driven technique has been used in the design of various circuits (Khameh & Shamsi, 2012, Stockstad & Yoshizawa, 2002; Zuo & Islam, 2013; Raj & Sharma, 2011; Gak, Miguez, & Arnaud, 2014) due to its simple architecture. However, the technique suffers from low gain due to body transconductance and also its large sensitivity to device mismatch and process variations. In contrast, BDFG/BDQFG approach (Khateb et al., 2013) improves the transconductance, i.e. effective transconductance is the sum of body transconductance and quasi-floating gate (QFG) transconductance. The QFG MOS transistors are wide-band ac coupled circuits. The capacitive divider network at gate terminal of QFG MOS transistor improves linearity of the device and using this attractive feature, few reported circuits included design of highly linear programmable CMOS OTA (Miguel, Lopez-Martin, Acosta, Ramirez-Angulo, & Carvajal, 2011), MOS resistor (Torralba et al., 2009), GM-C filter (Garcia-Alberdi, Lopez-Martin, Acosta, Carvajal, & Ramirez-Angulo, 2013), current conveyor (Moradzadeh & Azhari, 2011), current mirror (Gupta & Sharma, 2012; Raj, Singh, & Gupta, 2014) and many more. The experimental analysis of QFG emphasises its uses in low power designs (Ramirez-Angulo, Lopez-Martin, Carvajal, & Chavero, 2004). Combining the features of QFG with BD MOS transistors results in low power high-performance circuits. Studies have pointed to BDQFG technique (Khateb, 2014) as a better choice for realising low power circuits (Khateb, 2015; Raj, Singh, & Gupta, 2014a; Raj, Singh, & Gupta, 2016; Raj, Singh, & Gupta, 2016a). In this paper, to exploit the advantage of using BDQFG technique, design of a low voltage (LV) low power (LP) CCII using two-stage Miller compensated OTA is proposed. Analysis and simulation results indicate the proposed CCII suitable for high frequency low power applications. The paper is organised as follows: section 2 of the paper presents a brief discussion on BDQFG MOSFET followed by the design of CCII in section 3. The simulation results are shown in section 4 followed by conclusion in section 5.

BD and BDQFG Misfit

The MOSFET bulk terminal is usually connected to the most negative/positive supply voltage for N-channel/P-channel MOS transistor respectively. However, the bulk can also be used as secondary gate which removes the threshold voltage obstacle from input signal path. The first article based on BD technique was initially reported in (Guzinski, Bialko, & Matheau, 1987). The schematic of BD NMOS transistor is shown in Figure 1(a). The dc bias voltage V_{bias} at gate forms the channel whereas the applied input at bulk causes the drain-to-source current to flow. The main drawback with BD MOSFET has been its small body transconductance (g_{mb}) and degraded frequency response (Rosenfeld, Kozak, & Friedman, 2004). The body transconductance (g_{mb}) is related to gate transconductance (g_m) as

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f - V_{SB}}} g_m = \eta g_m \tag{1}$$

where γ is the body effect co-efficient, ϕ_f of is the fermi-potential, and V_{SB} is the source-to-bulk potential. The normal range of η varies from 0.2 to 0.4. In view to BD drawbacks, the BDQFG technique overcomes these issues without making significant effort. The BDQFG is the combination of architectures BD and quasi-floating gate (QFG). Under DC analysis it works

as simple BD whereas for AC it combines the features of BD and QFG MOS transistor. As a result, the transconductance and bandwidth are improved without changing the DC behaviour. The effective transconductance for BDQFG is given by

$$g_{m,BDQFG} = \frac{\left(C_{in} + C_{qfgb}\right)}{C_{T,qfg}} g_m + g_{mb} \tag{2}$$

where $C_{T,qfg} = C_{in} + C_{qfgb} + C_{gd,MP} + C_{qfgd} + C_{qfgs}$ is the total capacitance. The schematic of BDQFG MOSFET is shown in Figure 1 (b) where the bulk is tied to the gate input terminal of QFG MOSFET MN.

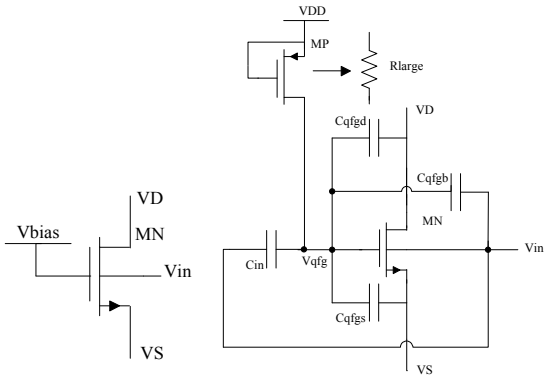

Figure 1. N-Channel: (a) BD; (b) BDQFG NMOS transistor. Adapted from "A survey of non-conventional techniques for low-voltage low-power analog circuit design," (Khateb., Dabbous., & Vlassis. (2013). *Radioengineering*, 22(2), p. 416,421, Copyright 2013 by Radioengineering

METHODOLOGY

Proposed positive type CCII

The CCII is a 3-port device firstly presented in (Sedra & Smith, 1970). The matrix representation of $CCII_{\pm}$ is given by

$$\begin{matrix} V_X \\ I_{Z\pm} \\ I_Y \end{matrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \pm 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z\pm} \end{bmatrix} \tag{3}$$

Where *X* and *Y* are the input terminals and *Z* + &*Z* are the output nodes. The ideal condition of CCII implies the *X* terminal should be at low impedance node whereas *Y*, *Z*+ and *Z*- should be at high impedance node. Few popular articles related to LV LP CCII design can be observed in (Khateb, Khatib, & Kubánek, 2011, Khateb, Khatib, & Kubánek, 2012 and Khateb, Khatib, & Kubánek, 2012a). The proposed LV LP positive CCII based on Miller compensated BD based and BDQFG based OTA is shown in Figure 2 and Figure 3 respectively.

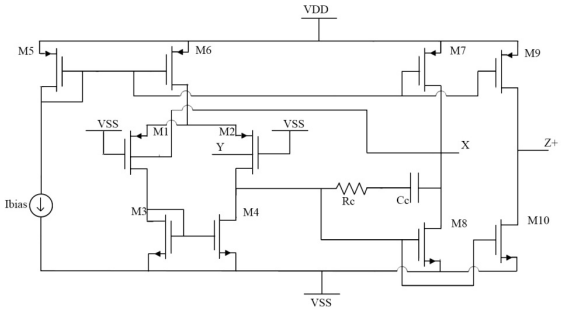

Figure 2. Proposed CCII+ based on BD Miller OTA

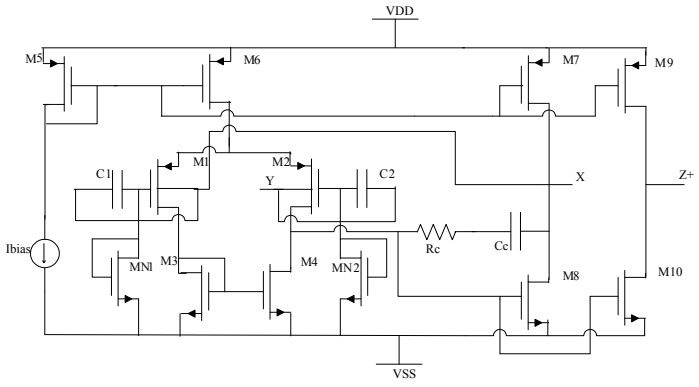

Figure 3. Proposed CCII+ based on BDQFG Miller OTA

The BDQFG technique is preferred over BD as it offers better performance at the same level of power consumption. The OTA is a voltage-controlled current source (VCCS) device whose ideal characteristics are high bandwidth and high input and output impedances (Lopez-Martin, Acosta, Algueta, Ramirez-Angulo, & Carvajal, 2009). The conventional bulk driven OTA suffers from limited linearity, low gain and bandwidth. The Miller OTA is realised using MOSFET (M1-M8) in both Figure 2 and Figure 3. The inputs to OTA are the BD MOSFET M1 and M2 in Figure 2. In Figure 3, the M1 and M2 in configured BDQFG MOSFET with the help of input capacitors C1 and C2 respectively. For making the gates of M1 and M2 quasi floating in Figure 3, these are connected with cut-off MOSFET MN1 and MN2 respectively. Rest of the configurations in both the OTA remains the same. The combination (M3, M4) and (M5, M6, M7) are simple current mirror architectures and the biasing current (I_{bias}) is used to bias the amplifier. The capacitor C_C is used as miller compensation which improves the phase response of OTA. However, due to feed forward path via miller capacitor, a zero is created in right half plane which degrades the phase shift of amplifier causing stability issues at high frequency, for which a null resistor (R_C) is used in series with miller capacitor which creates an extra pole to cancel the zero effect.

For CCII+ realisation, the positive input of OTA is considered as the Y-terminal of CCII+ whereas for X-terminal the OTA is configured in unity gain buffer mode by shorting the output

to the negative input terminal of OTA. This way it generates the positive type single output labelled as Z+ for CCII+.

RESULTS AND DISCUSSIONS

The proposed LV LP CCII+ of Figure 2 and Figure 3 are simulated on 0.18 μm mixed-mode twin-well technology using HSpice. The dimensions of MOSFET used in design for both CCII+ are shown in Table 1. The values of other parameters assumed for CCII+ are R_C = =10K, $C_C = C_1 = C_2$ = 1pf and a bias current I_{bias} of 10 μA. The simulation results of the proposed LV LP BD and BDQFG based CCII+ are shown in Figure 4 to Figure 9.

Table 1
Dimension of MOS transistors used in CCII+

MOSFETs	W (μm)	L (μm)	MOSFETs	W (μm)	L (μm)
M1	12	0.6	M7	8	0.6
M2	12	0.6	M8	23.9	0.6
M3	12	0.6	M9	8	0.6
M4	12	0.6	M10	23.9	0.6
M5	4	0.6	MN1	0.36	0.36
M6	9	0.6	MN2	0.36	0.36

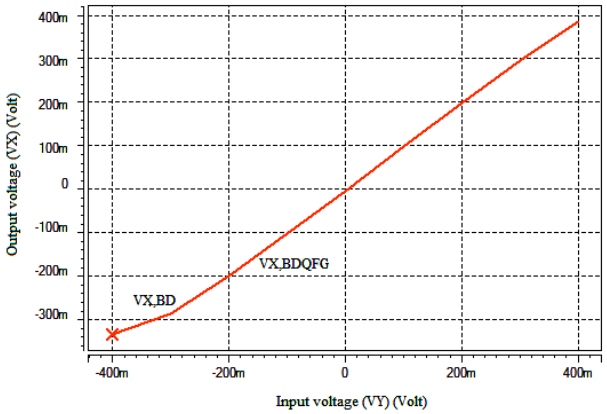

Figure 4. DC curve of $V_{X,BD}$ and $V_{X,BDQFG}$ versus V_Y

Figure 4 shows the DC transfer curve of V_X versus V_Y where V_X shows the signal swing from -0.3V to 0.3V. The current transfer curve for I_{Z+} as per Figure 5 shows the linear operation in the range of -20 μA to 20 μA with the minimal error. As observed under DC conditions, the characteristics of BD and BDQFG remain same so the identical characteristics are obtained in Figure 4 and Figure 5.

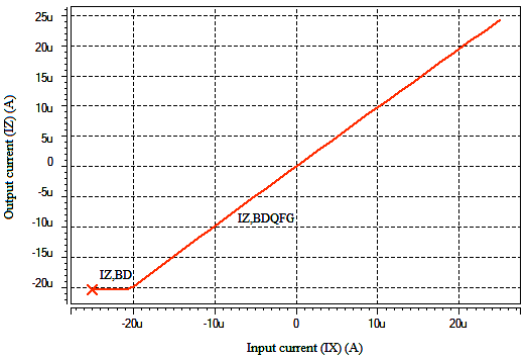

Figure 5. DC curves of $I_{Z,BD}$ and $I_{Z,BDQFG}$ with respect to I_X

The bandwidth response of I_z/I_x is shown in Figure 6. The observed bandwidth of I_z/I_x for BD CCII+ is 150MHz whereas for BDQFG CCII+ is found to be 400MHz. The high bandwidth encourages BDQFG CCII+ over BD CCII+ for high speed applications.

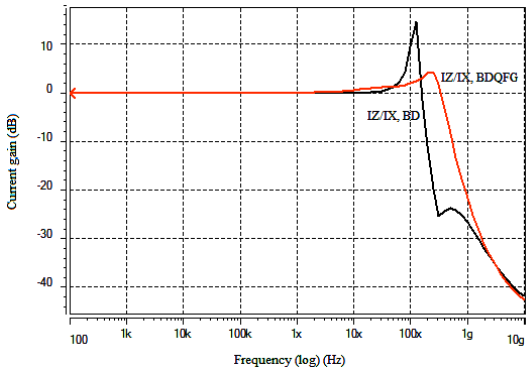

Figure 6. Frequency responses of current gain $\left(I_{Z+}/I_X\right)_{BD}$ and $\left(I_{Z+}/I_X\right)_{BDQFG}$

Figures 7 and 8 show the frequency dependence of the parasitic impedances of X and Z+ terminals. At low frequency impedance at X for BD CCII+ is 2.1Kohm whereas for BDQFG CCII+ is 450ohm. Similarly, the Z+ impedance is found as 115 $K\Omega$ for BD CCII+ and 115 $K\Omega$ for BDQFG CCII+.

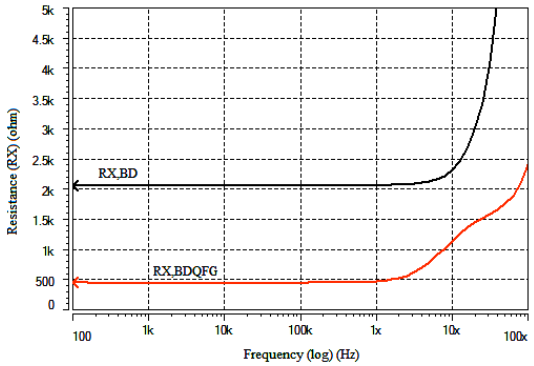

Figure 7. Parasitic impedance of *X* terminal

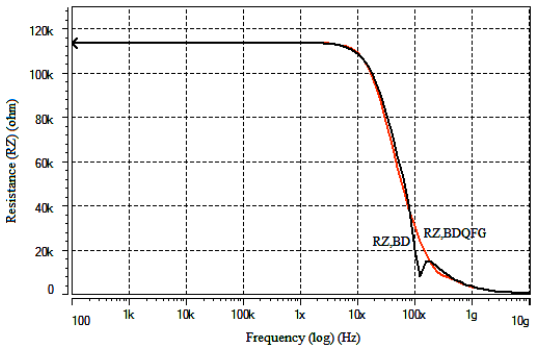

Figure 8. Parasitic impedance of *Z+* terminal

From above simulations, it can be easily concluded that when desired is low power circuits with better performance then BDQFG best fit to requirement since the power level consumption in both the techniques remains same. The complete simulation results for BD CCII+ and BDQFG CCII+ are summarised in Table 2.

Table 2
Comparison of Proposed BD and BDQFG based CCII+

Parameters	Proposed BD CCII+	Proposed BDQFG CCII+
DC voltage range (Vx)	-0.3V to +0.3V	-0.3V to +0.3V
DC Current range (Iz)	-20uA to +20uA	-20uA to +20uA
Current gain	1	1
Bandwidth (Iz/Ix)	150MHz	400MHz
RX (ohm)	2.1K	450
RZ (ohm)	115K	115K
Power	57.4uW	57.3uW
Supply	0.4V	0.4V
Technology	0.18 μm	0.18 μm

CONCLUSION

Various low voltage low power techniques have been reported in literature for design of low power circuits. Among existing techniques, the BD has gained considerable potential interest due to its simple structure. However, its sensitivity to device mismatch, poor gain and frequency performances puts its adaptability only to low gain and low frequency applications. Alternatively, using BDQFG as a replacement to BD improves the performances of BD technique which in this paper is shown with the help of design of positive second generation current conveyor.

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